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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,463	10/28/2003	Tadao Kishimoto	03648/HG	5626

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,463	KISHIMOTO ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 8* is/are rejected.

7)☒ Claim(s) *2,5-7 and 9-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1203 & 0605*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: NCIPI machine translation into English of JP2001-210922 A (5 pages).

DETAILED ACTION

Drawings

1. Figure 1(a), 1(b), 2, 3, 4, 5 and 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

On p.9, line 8: change "resister" to --resistor--.

On p.12, line 8: insert --is-- after "pattern".

On p.19, line 13: change the second occurrence of "12(a)" to --12(d)--.

On p.23, the bottom line: change "resister" to --resistor--.

On p.24, lines 4 and 5: change "snabber" to --snubber--.

On p.29, fourth line from the bottom: change "resister" to --resistor--.

3. Appropriate correction is required.

Claim Objections

4. Claims 2, 7, 8 and 12 are objected to because of the following informalities:

a) In Claim 2, line 3: change "resister" to --resistor--.

b) In Claims 7 and 12, lines 6-7, the insulation layer is recited as between the "inner area" and the "flat plane." This is not what is supported in the Specification. Consistent with the supporting disclosure (see Specification, p.26: the description of Fig. 12(d)), lines 6-7 of Claims 7 and 12 should be amended as follows:

(i) In line 6, change "a" to --an--.

(ii) In lines 6-7, "flat plane" should be changed to --multi-layer printed circuit board--.

c) In Claim 8, next-to-last line: insert --is-- after "pattern".

5. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Ito (JP2001-210922 A) [*Submitted by Applicant with IDS filed December 18, 2003. NCIPI machine translation into English was obtained and used by Examiner in the rejections hereinbelow and has been provided as an attachment to the instant Office Action*].

As to Claim 1, Ito discloses, in Fig. 7 (multilayer board 11 in Fig. 7 has same wiring configuration as multilayer board 11 in Fig. 2; paragraph [0013], wherein element 12 in Fig. 7 is the same power layer as element 3 in Fig. 1): first signal layer 4 (from Fig. 1) on an obverse surface of multilayer board 11; a ground layer 2 next to first signal layer 4; power layer 12 arranged next to ground layer 2 (from Figs. 2 and 7: both element 3 in Fig. 2 and element 12 in Fig. 7 are power layers); a second signal layer 5 (from Fig. 1) on a reverse side of multilayer board 11; a first ground pattern 7 is formed around a peripheral area of first signal layer 4 and a second ground pattern 8 is formed around a peripheral area of second signal layer 5 (Figs. 3_1, 3_4; paragraph [0013]); first ground pattern 7 and second ground pattern 8 are electrically coupled by through-holes 9 (paragraph [0013]), multilayer board 11 is installed on an electro-conductive housing (comprising elements 16 and 17; paragraph [0017]) in such a manner that a substantially whole area of second ground pattern 8 (Fig. 3_4) **electrically** contacts (i.e., by way of conductive through-holes 9, first ground pattern 7 and conductive posts 15; paragraph [0015]-[0017]) a mounting area (i.e., bent portion of element 16) of the electro-conductive housing), the mounting area being an electro-conductive area continuously coupled to the electro-conductive housing (housing mounting element 16 is electrically and mechanically coupled to housing element 18 by screws; Fig. 7 and paragraph [0017]).

As to Claim 8, Ito discloses, in Figs. 9 and 10, (multilayer board 11 in Fig. 9 has same wiring configuration as multilayer board 11 in Figs. 2 and 7; paragraph [0013]): a method for installing a multilayer PCB on an electro-conductive housing 6, the multi-

layer PCB, on which electronic parts 31 are mounted (paragraph [0022]) comprising: a first signal layer 4 (from Fig. 1) formed on an obverse surface of multilayer PCB 11, a ground layer 2 arranged at a position next to first signal layer 4, a power layer 12 arranged at a position next to ground layer 2 (from Figs. 2 and 7: both element 3 in Fig. 2 and element 12 in Fig. 7 are power layers), and a second signal layer 5 formed on a reverse surface of multilayer PCB 11, the method comprising the steps of: forming a ground pattern 7 around a peripheral area of first signal layer 4 and forming a ground pattern 8 around a peripheral area of second signal layer 5 (Figs. 3_1 and 3_4; paragraph [0013]) electrically coupling first ground pattern 7 to second ground pattern 8 with a plurality of through-holes 9 (Fig. 9; paragraph [0013]); mounting multilayer PCB 11 on a mounting area (side walls) of electro-conductive housing 6 in such a manner that a substantially whole area of first ground pattern 7 is **electrically** coupled to electro-conductive housing 6 through an electro-conductive member 37 (Figs. 9 and 10; paragraph [0023]).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito (JP2001-210922 A) [*Submitted by Applicant with IDS filed December 18, 2003. NCIPI machine translation into English was obtained and used by Examiner in the rejections hereinbelow and has been provided as an attachment to the instant Office Action*].

A) As to Claim 3:

I. Ito discloses, in Fig. 7, (multilayer board 11 has same wiring configuration as multilayer board 11 in Fig. 2; paragraph [0013]): a method for installing a multilayer PCB on an electro-conductive housing (comprising housing elements 16 and 17; paragraph [0017]), the multi-layer PCB comprising: a first signal layer 4 (from Fig. 1) formed on an obverse surface of multilayer PCB 11, a ground layer 2 arranged at a position next to first signal layer 4, a power layer 12 arranged at a position next to ground layer 2 (from Figs. 2 and 7: both element 3 in Fig. 2 and element 12 in Fig. 7 are power layers), and a second signal layer 5 formed on a reverse surface of multilayer PCB 11, the method comprising the steps of: forming a ground pattern 7 around a peripheral area of first signal layer 4 and forming a ground pattern 8 around a peripheral area of second signal

layer 5 (Figs. 3_1 and 3_4; paragraph [0013]) electrically coupling first ground pattern 7 to second ground pattern 8 with a plurality of through-holes 9 (Fig. 9; paragraph [0013]); mounting multilayer PCB 11 on a mounting area (i.e., bent portion of housing element 16) of the electro-conductive housing (paragraph [0017]) in such a manner that a substantially whole area of second ground pattern 8 (Fig. 3_4) **electrically** contacts (i.e., by way of conductive through-holes 9, first ground pattern 7 and conductive posts 15; paragraph [0015]-[0017]) the mounting area (i.e., bent portion of housing mounting element 16) of the electro-conductive housing, the mounting area being an electro-conductive area continuously coupled to the electro-conductive housing (housing mounting element 16 is electrically and mechanically coupled to housing element 18 by screws; Fig. 7 and paragraph [0017]).

II. Ito does not depict electronic parts mounted on PCB 11 in the embodiment of Fig. 7. However, Ito teaches the EMI problems of a functional circuit board with shielding and mounted in electronic equipment (paragraphs [0002] and [0008]) and it is old and well-known in the art to provide functionality to a circuit board by mounting electronic parts, such as IC chips for memory, processor, controller, etc. for performing electronic functions and/or passive parts such as resistors and capacitors for conditioning and filtering the signals. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add any electronic parts to PCB 11 required for performing the functions in the electronic equipment in which the PCB is mounted.

B) As to Claim 4:

I. Ito further discloses the mounting area of the electro-conductive housing is formed in a protruded shape (i.e., mounting element 16 containing the mounting portion protrudes from housing element 17; see Fig. 7).

II. Ito does not explicitly depict the electronic parts in the embodiment of Fig. 7 but does depict electronic parts in the similar package assembly in the embodiment of Fig. 9, wherein electronic parts 31 are mounted on the signal layer 4 such that the electronic parts 31 are held by multilayer PCB 11 without physically touching the electro-conductive housing (Fig. 7). Since Ito discloses various embodiments of the invention for use in the same electronic equipment applications, then the mounting of electronic parts 31 on the signal layer 4 of Fig. 7 would have been obvious to one of ordinary skill in the art at the time the invention was made for the same purpose of providing a functionality required by the application as in the embodiment of Fig. 9.

Allowable Subject Matter

11. Claims 2, 5-7 and 9-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Harada et al. (US 6,198,362 B1) discloses snubber (series RC) circuits distributed around the periphery of the multilayer board (with outer signal layers 24a,b and inner ground and power layers 22 and 23; col.8: 35-40) in order to suppress EM radiation from the board (Figs. 7 and 8; col.8: 41-67), the snubber circuits enabling EM radiation suppression without costly and bulky EM shields and the use of special board design for use with the EM shields (col.1: 22-55; col.2: 40-49).

Harada et al. (US 6,198,362 B1) discloses snubber (series RC) circuits distributed around the periphery of the multilayer board (with outer signal layers 44 and inner ground and power layers 42 and 43; col.15: 6-10) in order to suppress EM radiation from the board (Figs. 22 and 23; col.15: 13-19 and 50-67), the snubber circuits enabling EM radiation suppression without costly and bulky EM shields and the use of special board design for use with the EM shields (col.3: 1-55).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
October 17, 2005